PCA9512A

Level shifting hot swappable I²C-bus and SMBus bus buffer

Rev. 01 — 7 October 2005 Product data sheet

1. General description

The PCA9512A is a hot swappable I²C-bus and SMBus buffer that allows I/O card insertion into a live backplane without corruption of the data and clock buses and includes two dedicated supply voltage pins to provide level shifting between 3.3 V and 5 V systems while maintaining the best noise margin for each voltage level. Either pin may be powered with supply voltages ranging from 2.7 V to 5.5 V with no constraints on which supply voltage is higher. Control circuitry prevents the backplane from being connected to the card until a stop bit or bus idle occurs on the backplane without bus contention on the card. When the connection is made, the PCA9512A provides bidirectional buffering, keeping the backplane and card capacitances isolated.

The PCA9512A rise time accelerator circuitry allows the use of weaker DC pull-up currents while still meeting rise time requirements. The PCA9512A incorporates a digital input pin that enables and disables the rise time accelerators on all four SDAn and SCLn pins.

During insertion, the PCA9512A SDAn and SCLn pins are precharged to 1 V to minimize the current required to charge the parasitic capacitance of the chip.

The dynamic offset design of the PCA9510A/11A/12A/13A/14A I/O drivers allow them to be connected to another PCA9510A/11A/12A/13A/14A device in series or in parallel and to the A side of the PCA9517. The PCA9510A/11A/12A/13A/14A **cannot** connect to the static offset I/Os used on the PCA9515/15A/16/16A/18, PCA9517 B side, or P82B96 Sx/y side.

2. Features

- Bidirectional buffer for SDA and SCL lines increases fanout and prevents SDA and SCL corruption during live board insertion and removal from multi-point backplane systems
- Compatible with I²C-bus Standard mode, I²C-bus Fast mode, and SMBus standards
- Built-in $\Delta V/\Delta t$ rise time accelerators on all SDAn and SCLn pins (0.6 V threshold) with ability to disable $\Delta V/\Delta t$ rise time accelerator through the ACC pin for lightly loaded systems
- 5 V to 3.3 V level translation with optimum noise margin
- High-impedance SDAn and SCLn pins for V_{CC} or V_{CC2} = 0 V
- 1 V precharge on all SDAn and SCLn pins
- Supports clock stretching and multiple master arbitration and synchronization
- Operating power supply voltage range: 2.7 V to 5.5 V
- I/Os are not 5.5 V tolerant
- 0 Hz to 400 kHz clock frequency

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- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO8, TSSOP8 (MSOP8)

3. Applications

- cPCI, VME, AdvancedTCA cards and other multi-point backplane cards that are required to be inserted or removed from an operating system

4. Feature selection

Table 1: Feature selection chart

Feature	PCA9510A	PCA9511A	PCA9512A	PCA9513A	PCA9514A
Idle detect	yes	yes	yes	yes	yes
High-impedance SDAn, SCLn pins for V_{CC} = 0 V	yes	yes	yes	yes	yes
Rise time accelerator circuitry on SDAn and SCLn pins	-	yes	yes	yes	yes
Rise time accelerator circuitry hardware disable pin for lightly loaded systems	-	-	yes	-	-
Rise time accelerator threshold 0.8 V versus 0.6 V improves noise margin	-	-	-	yes	yes
Ready open-drain output	yes	yes	-	yes	yes
Two V_{CC} pins to support 5 V to 3.3 V level translation with improved noise margins	-	-	yes	-	-
1 V precharge on all SDAn and SCLn pins	in only	yes	yes	-	-
92 µA current source on SCLIN and SDAIN for PICMG applications	-	-	-	yes	-

5. Ordering information

Table 2: Ordering information

T_{amb} = −40 °C to +85 °C

Type number	Topside mark	Package		
		Name	Description	Version
PCA9512AD	PA9512A	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
PCA9512ADP	9512A	TSSOP8 [1]	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1

[1] Also known as MSOP8.

Standard packing quantities and other packaging data are available at the Philips website.

6. Block diagram

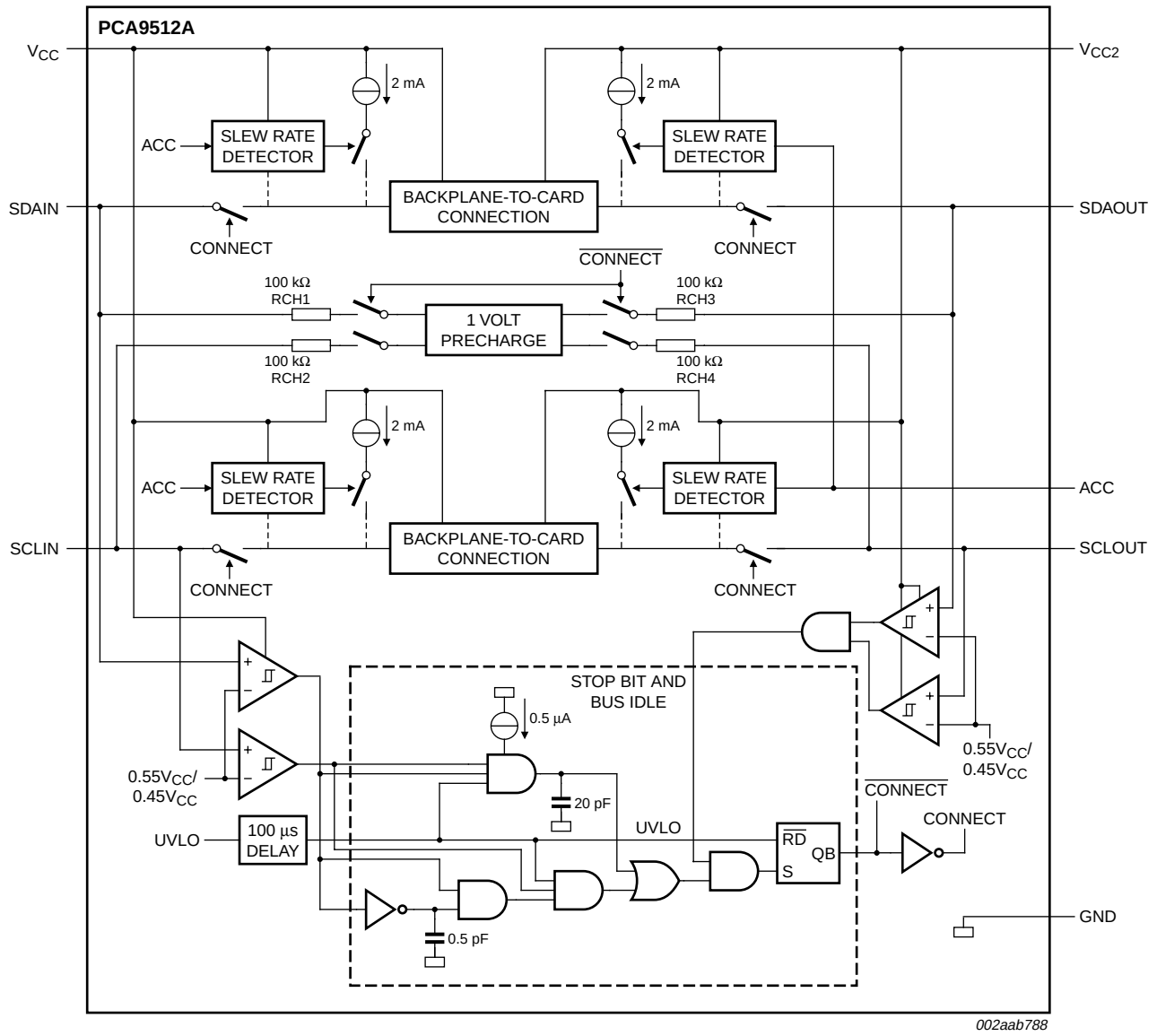


Fig 1. Block diagram of PCA9512A

7. Pinning information

7.1 Pinning

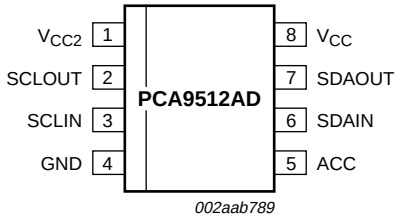


Fig 2. Pin configuration for SO8

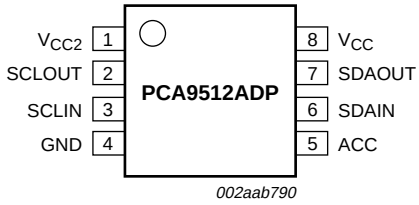


Fig 3. Pin configuration for TSSOP8

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
V_{CC2}	1	Supply voltage for devices on the card I²C-buses. Connect pull-up resistors from SDAOUT and SCLOUT to this pin.
SCLOUT	2	serial clock output to and from the SCL bus on the card
SCLIN	3	serial clock input to and from the SCL bus on the backplane
GND	4	ground supply; connect this pin to a ground plane for best results.
ACC	5	CMOS threshold digital input pin that enables and disables the rise time accelerators on all four SDAn and SCLn pins. ACC enables all accelerators when set to V_{CC2}, and turns them off when set to GND.
SDAIN	6	serial data input to and from the SDA bus on the backplane
SDAOUT	7	serial data output to and from the SDA bus on the card
V_{CC}	8	supply voltage; from the backplane, connect pull-up resistors from SDAIN and SCLIN to this pin.

8. Functional description

Refer to Figure 1 “Block diagram of PCA9512A”.

8.1 Start-up

When the PCA9512A is powered up, either V_{CC} or V_{CC2} may rise first and either may be more positive or they may be equal, however the PCA9512A will not leave the undervoltage lock out or initialization state until both V_{CC} and V_{CC2} have gone above 2.5 V. If either V_{CC} or V_{CC2} drops below 2.0 V it will return to the undervoltage lock out state. In the undervoltage lock out state the connection circuitry is disabled, the rise time accelerators are disabled, and the precharge circuitry is also disabled. After both V_{CC} and V_{CC2} are valid, independent of which is higher, the PCA9512A enters the initialization state; during this state the 1 V precharge circuitry is activated and pulls up the SDAn and SCLn pins to 1 V through individual 100 kΩ nominal resistors. At the end of the initialization state the ‘Stop bit and bus idle’ detect circuit is enabled. When all the SDAn and SCLn pins have been HIGH for the bus idle time or when all pins are HIGH and a

STOP condition is seen on the SDAIN and SCLIN pins, the connect circuitry is activated, connecting SDAIN to SDAOUT and SCLIN to SCLOUT. The 1 V precharge circuitry is disabled when the connection is made, unless the ACC pin is LOW; the rise time accelerators are enabled at this time also.

8.2 Connect circuitry

Once the connection circuitry is activated, the behavior of SDAIN and SDAOUT as well as SCLIN and SCLOUT become identical, with each acting as a bidirectional buffer that isolates the input bus capacitance from the output bus capacitance while communicating. If $V_{CC} \neq V_{CC2}$, then a level shifting function is performed between input and output. A LOW forced on either SDAIN or SDAOUT will cause the other pin to be driven to a LOW by the PCA9512A. The same is also true for the SCLn pins. Noise between $0.7V_{CC}$ and V_{CC} on the SDAIN and SCLIN pins, and $0.7V_{CC2}$ and V_{CC2} on the SDAOUT and SCLOUT pins is generally ignored because a falling edge is only recognized when it falls below $0.7V_{CC}$ for SDAIN and SCLIN (or $0.7V_{CC2}$ for SDAOUT and SCLOUT pins) with a slew rate of at least 1.25 V/µs. When a falling edge is seen on one pin, the other pin in the pair turns on a pull-down driver that is referenced to a small voltage above the falling pin. The driver will pull the pin down at a slew rate determined by the driver and the load. The first falling pin may have a fast or slow slew rate; if it is faster than the pull-down slew rate, then the initial pull-down rate will continue until it is LOW. If the first falling pin has a slow slew rate, then the second pin will be pulled down at its initial slew rate only until it is just above the first pin voltage then they will both continue down at the slew rate of the first.

Once both sides are LOW they will remain LOW until all the external drivers have stopped driving LOWs. If both sides are being driven LOW to the same (or nearly the same) value by external drivers, which is the case for clock stretching and is typically the case for acknowledge, and one side external driver stops driving, that pin will rise and rise above the nominal offset voltage until the internal driver catches up and pulls it back down to the offset voltage. This bounce is worst for low capacitances and low resistances, and may become excessive. When the last external driver stops driving a LOW, that pin will bounce up and settle out just above the other pin as both rise together with a slew rate determined by the internal slew rate control and the RC time constant. As long as the slew rate is at least 1.25 V/µs, when the pin voltage exceeds 0.6 V, the rise time accelerator circuits are turned on and the pull-down driver is turned off. If the ACC pin is LOW, the rise time accelerator circuits will be disabled, but the pull-down driver will still turn off.

8.3 Maximum number of devices in series

Each buffer adds about 0.1 V dynamic level offset at 25 °C with the offset larger at higher temperatures. Maximum offset (V_{offset}) is 0.150 V with a 10 kΩ pull-up resistor. The LOW level at the signal origination end (master) is dependent upon the load and the only specification point is the I²C-bus specification of 3 mA will produce $V_{OL} < 0.4$ V, although if lightly loaded the V_{OL} may be ~0.1 V. Assuming $V_{OL} = 0.1$ V and $V_{offset} = 0.1$ V, the level after four buffers would be 0.5 V, which is only about 0.1 V below the threshold of the rising edge accelerator (about 0.6 V). With great care a system with four buffers may work, but as the V_{OL} moves up from 0.1 V, noise or bounces on the line will result in firing the rising edge accelerator thus introducing false clock edges. Generally it is recommended to limit the number of buffers in series to two, and to keep the load light to minimize the offset.

The PCA9510A (rise time accelerator is permanently disabled) and the PCA9512A (rise time accelerator can be turned off) are a little different with the rise time accelerator turned off because the rise time accelerator will not pull the node up, but the same logic that turns on the accelerator turns the pull-down off. If the V_{IL} is above ~0.6 V and a rising edge is detected, the pull-down will turn off and will not turn back on until a falling edge is detected.

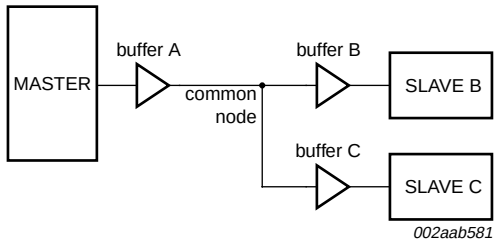


Fig 4. System with 3 buffers connected to common node

Consider a system with three buffers connected to a common node and communication between the Master and Slave B that are connected at either end of buffer A and buffer B in series as shown in Figure 4. Consider if the V_{OL} at the input of buffer A is 0.3 V and the V_{OL} of Slave B (when acknowledging) is 0.4 V with the direction changing from Master to Slave B and then from Slave B to Master. Before the direction change you would observe V_{IL} at the input of buffer A of 0.3 V and its output, the common node, is ~0.4 V. The output of buffer B and buffer C would be ~0.5 V, but Slave B is driving 0.4 V, so the voltage at Slave B is 0.4 V. The output of buffer C is ~0.5 V. When the Master pull-down turns off, the input of buffer A rises and so does its output, the common node, because it is the only part driving the node. The common node will rise to 0.5 V before buffer B's output turns on, if the pull-up is strong the node may bounce. If the bounce goes above the threshold for the rising edge accelerator ~0.6 V the accelerators on both buffer A and buffer C will fire contending with the output of buffer B. The node on the input of buffer A will go HIGH as will the input node of buffer C. After the common node voltage is stable for a while the rising edge accelerators will turn off and the common node will return to ~0.5 V because the buffer B is still on. The voltage at both the Master and Slave C nodes would then fall to ~0.6 V until Slave B turned off. This would not cause a failure on the data line as long as the return to 0.5 V on the common node (~0.6 V at the Master and Slave C) occurred before the data setup time. If this were the SCL line, the parts on buffer A and buffer C would see a false clock rather than a stretched clock, which would cause a system error.

8.4 Propagation delays

The delay for a rising edge is determined by the combined pull-up current from the bus resistors and the rise time accelerator current source and the effective capacitance on the lines. If the pull-up currents are the same, any difference in rise time is directly proportional to the difference in capacitance between the two sides. The t_{PLH} may be negative if the output capacitance is less than the input capacitance and would be positive if the output capacitance is larger than the input capacitance, when the currents are the same.

The t_{PHL} can never be negative because the output does not start to fall until the input is below $0.7V_{CC}$ (or $0.7V_{CC2}$ for SDAOUT and SCLOUT), and the output turn on has a non-zero delay, and the output has a limited maximum slew rate, and even if the input slew

rate is slow enough that the output catches up it will still lag the falling voltage of the input by the offset voltage. The maximum t_{PHL} occurs when the input is driven LOW with zero delay and the output is still limited by its turn-on delay and the falling edge slew rate. The output falling edge slew rate is a function of the internal maximum slew rate which is a function of temperature, V_{CC} or V_{CC2} and process, as well as the load current and the load capacitance.

8.5 Rise time accelerators

During positive bus transactions, a 2 mA current source is switched on to quickly slew the SDA and SCL lines HIGH once the input level of 0.6 V for the PCA9512A is exceeded. The rising edge rate should be at least 1.25 V/µs to guarantee turn on of the accelerators.

8.6 ACC boost current enable

Users having lightly loaded systems may wish to disable the rise time accelerators. Driving this pin to ground turns off the rise time accelerators on all four SDAn and SCLn pins. Driving this pin to the V_{CC2} voltage enables normal operation of the rise time accelerators.

8.7 Resistor pull-up value selection

The system pull-up resistors must be strong enough to provide a positive slew rate of 1.25 V/µs on the SDAn and SCLn pins, in order to activate the boost pull-up currents during rising edges. Choose maximum resistor value using the formula:

$$R_{PU} \leq 800 \times 10^3 \left(\frac{V_{CC(min)} - 0.6}{C} \right)$$

where R_{PU} is the pull-up resistor value in Ω, $V_{CC(min)}$ is the minimum V_{CC} voltage in volts, and C is the equivalent bus capacitance in picofarads.

In addition, regardless of the bus capacitance, always choose $R_{PU} \leq 16$ kΩ for $V_{CC} = 5.5$ V maximum, $R_{PU} \leq 24$ kΩ for $V_{CC} = 3.6$ V maximum. The start-up circuitry requires logic HIGH voltages on SDAOUT and SCLOUT to connect the backplane to the card, and these pull-up values are needed to overcome the precharge voltage. See the curves in Figure 5 and Figure 6 for guidance in resistor pull-up selection.

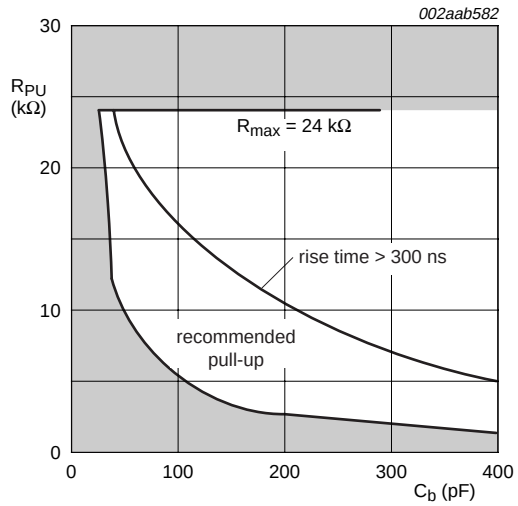


Fig 5. Bus requirements for 3.3 V systems

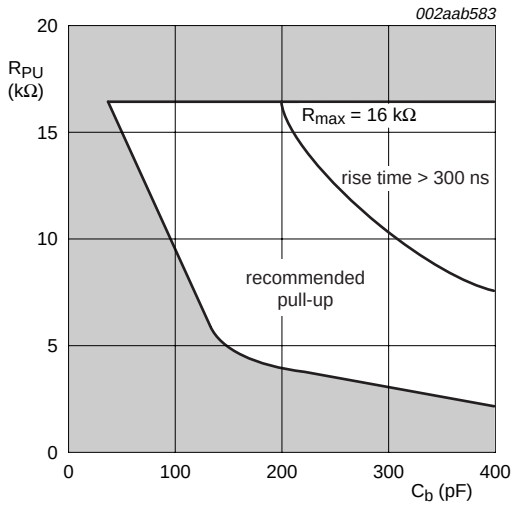
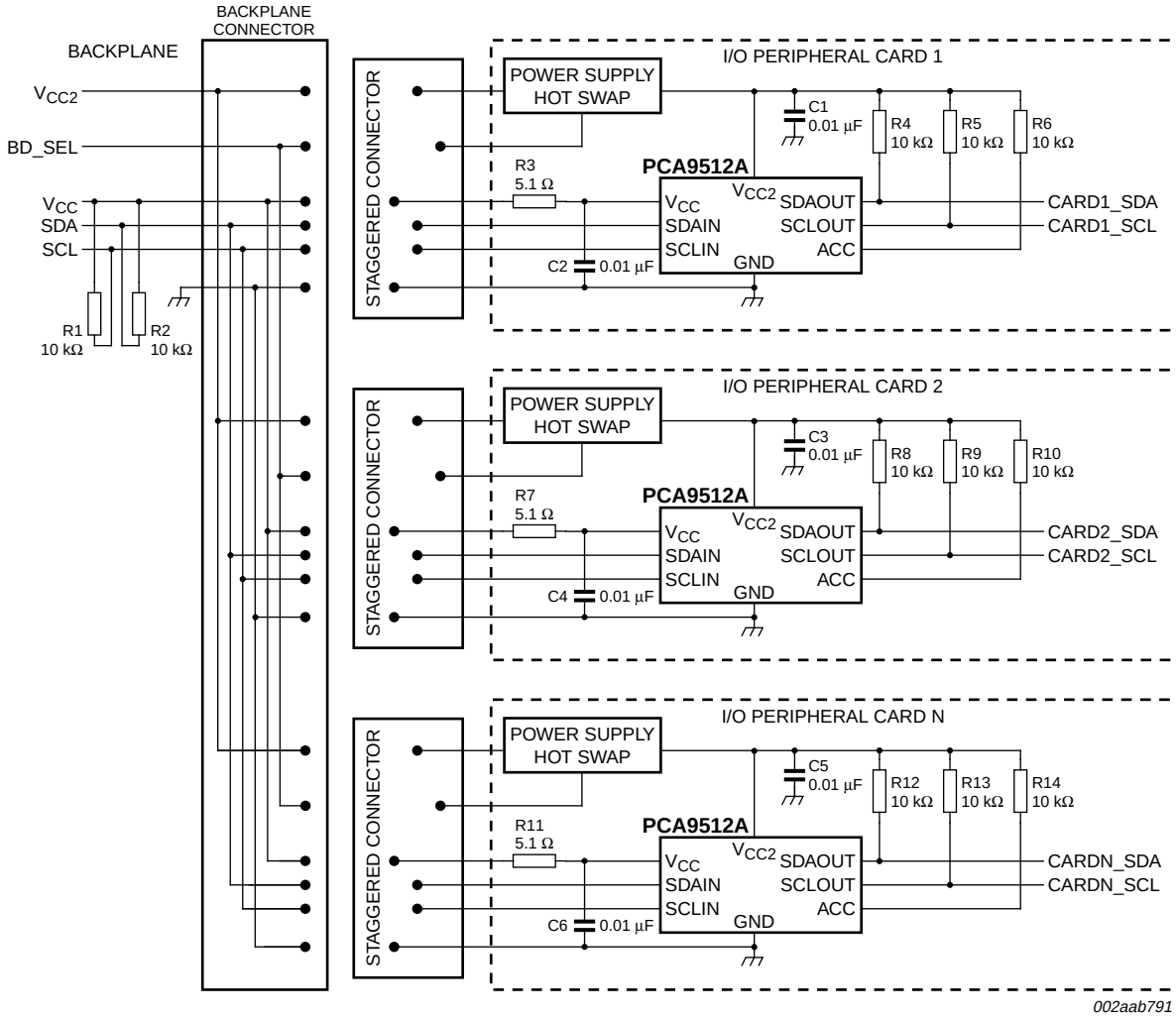


Fig 6. Bus requirements for 5 V systems

8.8 Hot swapping and capacitance buffering application

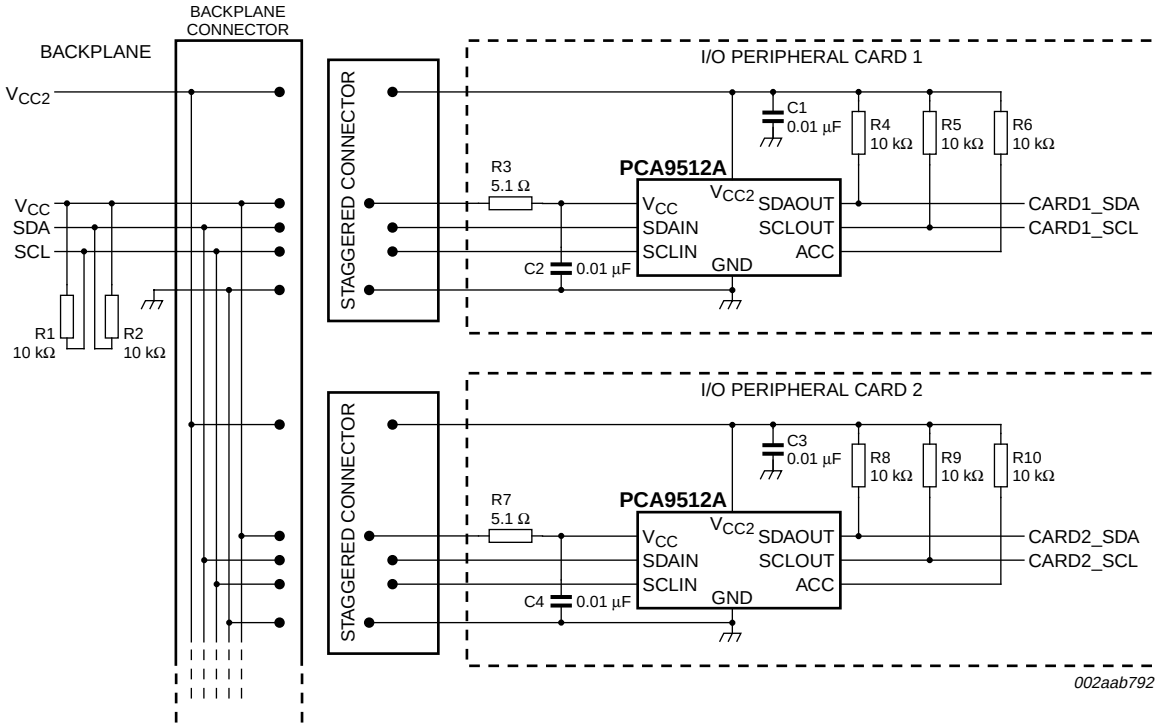
Figure 7 through Figure 9 illustrate the usage of the PCA9512A in applications that take advantage of both its hot swapping and capacitance buffering features. In all of these applications, note that if the I/O cards were plugged directly into the backplane, all of the backplane and card capacitances would add directly together, making rise time and fall time requirements difficult to meet. Placing a bus buffer on the edge of each card, however, isolates the card capacitance from the backplane. For a given I/O card, the PCA9512A drives the capacitance of everything on the card and the backplane must drive only the capacitance of the bus buffer, which is less than 10 pF, the connector, trace, and all additional cards on the backplane.

See *Application Note AN10160, 'Hot Swap Bus Buffer'* for more information on applications and technical assistance.



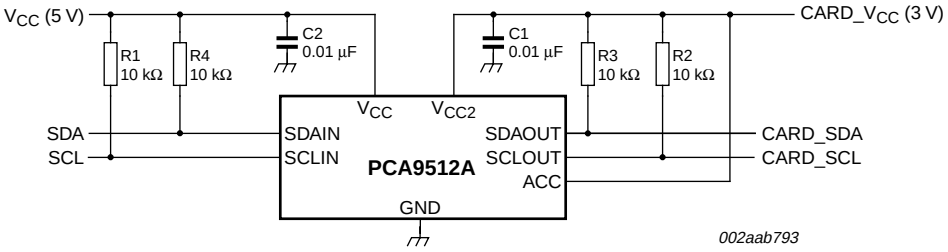
Remark: Application assumes bus capacitance within 'proper operation' region of Figure 5 and Figure 6.

Fig 7. Hot swapping multiple I/O cards into a backplane using the PCA9512A in a cPCI, VME, and AdvancedTCA system



Remark: Application assumes bus capacitance within 'proper operation' region of Figure 5 and Figure 6.

Fig 8. Hot swapping multiple I/O cards into a backplane using the PCA9512A with a custom connector



Remark: Application assumes bus capacitance within 'proper operation' region of Figure 5 and Figure 6.

Fig 9. 5 V to 3.3 V level translator and bus buffer

9. Application design-in information

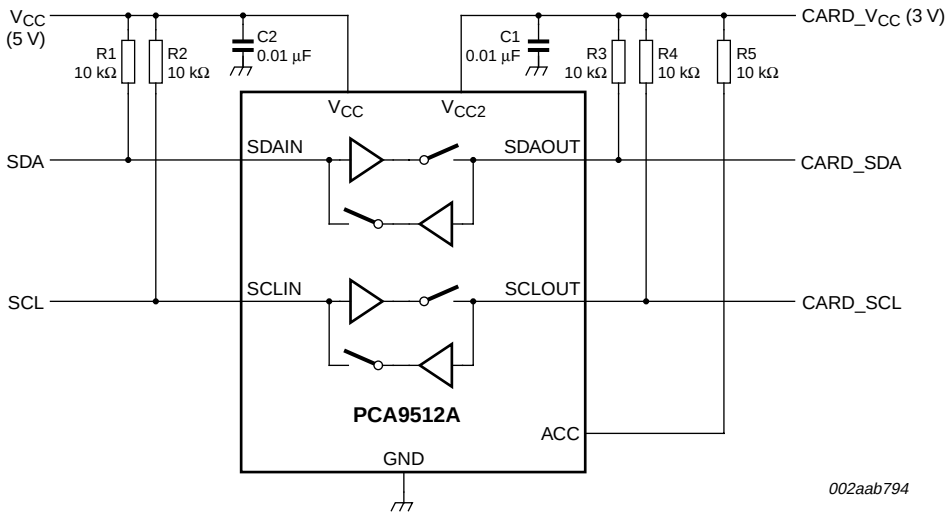


Fig 10. Typical application

10. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7	V
V_{CC2}	supply voltage 2 [1]			–0.5	+7	V
V_n	voltage on any other pin			–0.5	+7	V
I_I	input current		[2]	-	±20	mA
$I_{I/O}$	input/output current		[3]	-	±50	mA
T_{oper}	operating temperature			–40	+85	°C
T_{stg}	storage temperature			–65	+125	°C
T_{sp}	solder point temperature	10 s maximum		-	300	°C
$T_{j(max)}$	maximum junction temperature			-	125	°C

[1] Card side supply voltage.

[2] Maximum current for inputs.

[3] Maximum current for I/O pins.

11. Characteristics

Table 5: Characteristics

V_{CC} = 2.7 V to 5.5 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Power supply							
V_{CC}	supply voltage		[1]	2.7	-	5.5	V
V_{CC2}	supply voltage 2 [2]		[1]	2.7	-	5.5	V
I_{CC}	supply current	V_{CC} = 5.5 V; V_{SDAIN} = V_{SCLIN} = 0 V		-	1.8	3.6	mA
I_{CC2}	supply current 2	V_{CC} = 5.5 V; V_{SDAOUT} = V_{SCLOUT} = 0 V		-	1.7	2.9	mA
Start-up circuitry							
V_{pch}	precharge voltage	SDA, SCL floating	[1]	0.8	1.1	1.2	V
t_{en}	enable time	on power-up	[3]	-	180	-	µs
t_{idle}	idle time		[1] [4]	50	140	250	µs
Rise time accelerators							
$I_{trt(pu)}$	transient boosted pull-up current	positive transition on SDA, SCL; V_{ACC} = 0.7 × V_{CC2}; V_{CC} = 2.7 V; slew rate = 1.25 V/µs	[5]	1	2	-	mA
$V_{th(dis)(ACC)}$	disable threshold voltage on pin ACC			0.3V_{CC2}	0.5V_{CC2}	-	V
$V_{th(en)(ACC)}$	enable threshold voltage on pin ACC			-	0.5V_{CC2}	0.7V_{CC2}	V
$I_{I(ACC)}$	input current on pin ACC			−1	±0.1	+1	µA
$t_{PD(on/off)(ACC)}$	on/off propagation delay on pin ACC			-	5	-	ns
Input-output connection							
V_{offset}	offset voltage	10 kΩ to V_{CC} on SDA, SCL; V_{CC} = 3.3 V; V_{CC2} = 3.3 V; V_I = 0.2 V	[1] [6]	0	115	175	mV
C_i	input capacitance	digital; guaranteed by design, not subject to test		-	-	10	pF
V_{OL}	LOW-state output voltage	V_I = 0 V; SDAn, SCLn pins; I_{sink} = 3 mA; V_{CC} = 2.7 V; V_{CC2} = 2.7 V	[1]	0	0.3	0.4	V
I_{LI}	input leakage current	SDAn, SCLn pins; V_{CC} = 5.5 V; V_{CC2} = 5.5 V		−1	-	+1	µA

Table 5: Characteristics *...continued*

V_{CC} = 2.7 V to 5.5 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
System characteristics							
f_{SCL}	SCL clock frequency		[7]	0	-	400	kHz
t_{BUF}	bus free time between STOP condition and START condition		[7]	1.3	-	-	µs
$t_{HD;STA}$	START condition hold time		[7]	0.6	-	-	µs
$t_{SU;STA}$	START condition (or repeated START condition) set-up time		[7]	0.6	-	-	µs
$t_{SU;STO}$	STOP condition set-up time		[7]	0.6	-	-	µs
$t_{HD;DAT}$	data hold time		[7]	300	-	-	ns
$t_{SU;DAT}$	data set-up time		[7]	100	-	-	ns
t_{LOW}	SCL LOW time		[7]	1.3	-	-	µs
t_{HIGH}	SCL HIGH time		[7]	0.6	-	-	µs
t_f	fall time SDA and SCL		[7] [8]	$20 + 0.1 \times C_b$	-	300	ns
t_r	rise time SDA and SCL		[7] [8]	$20 + 0.1 \times C_b$	-	300	ns

[1] This specification applies over the full operating temperature range.

[2] Card side supply voltage.

[3] The enable time is from power-up of V_{CC} and $V_{CC2} \geq 2.7$ V to when idle or stop time begins.

[4] Idle time is from when SDAn and SCLn are HIGH after enable time has been met.

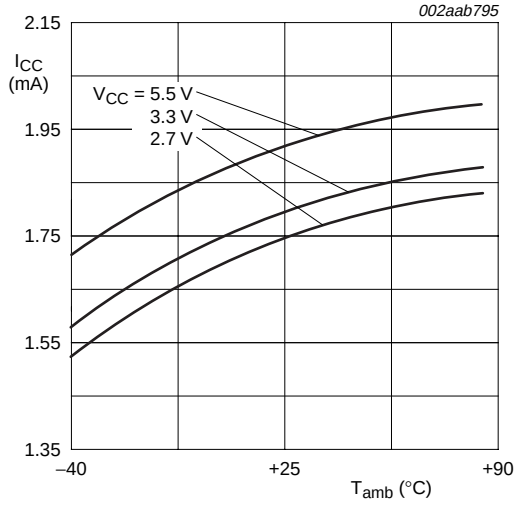
[5] $I_{trt(pu)}$ varies with temperature and V_{CC} voltage, as shown in Section 11.1 “Typical performance characteristics”.

[6] The connection circuitry always regulates its output to a higher voltage than its input. The magnitude of this offset voltage as a function of the pull-up resistor and V_{CC} voltage is shown in Section 11.1 “Typical performance characteristics”.

[7] Guaranteed by design, not production tested.

[8] C_b = total capacitance of one bus line in pF.

11.1 Typical performance characteristics



I_{CC2} (pin 1) typical current averages 0.1 mA less than I_{CC} on pin 8.

Fig 11. I_{CC} versus temperature

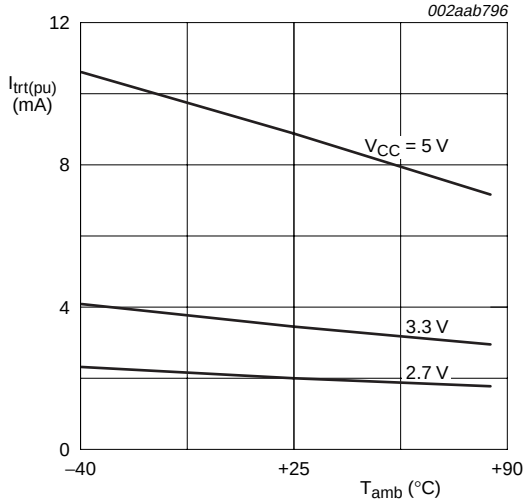
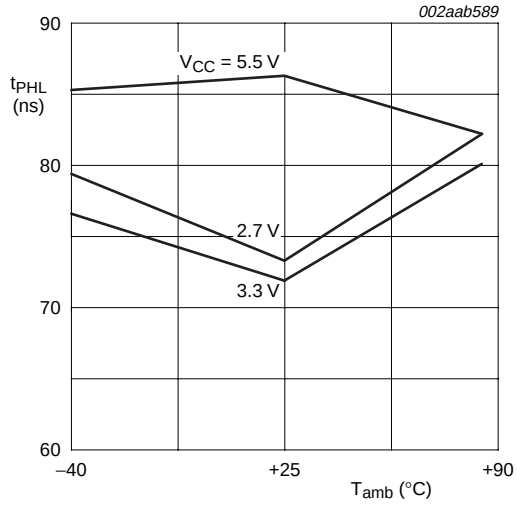
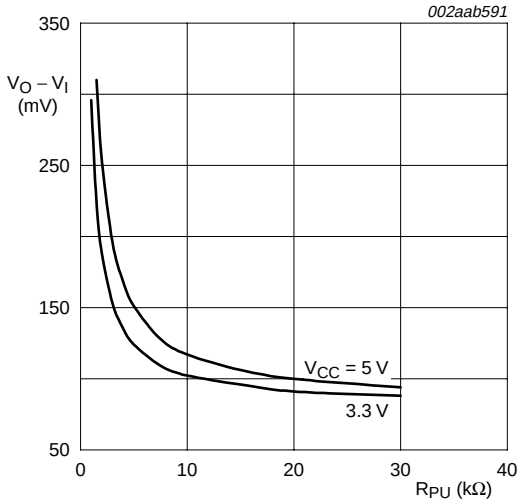


Fig 12. $I_{trt(pu)}$ versus temperature



$C_i = C_o > 100$ pF; $R_{PU(in)} = R_{PU(out)} = 10$ kΩ

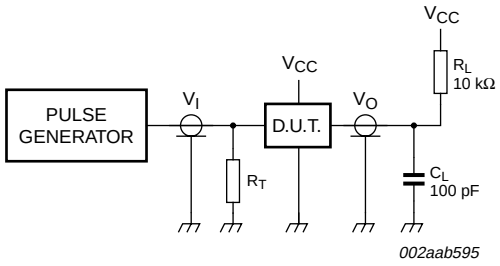
Fig 13. Input/output t_{PHL} versus temperature



V_{CC} = 3.3 V or 5.5 V

Fig 14. Connection circuitry $V_O - V_I$

12. Test information



R_L = load resistor

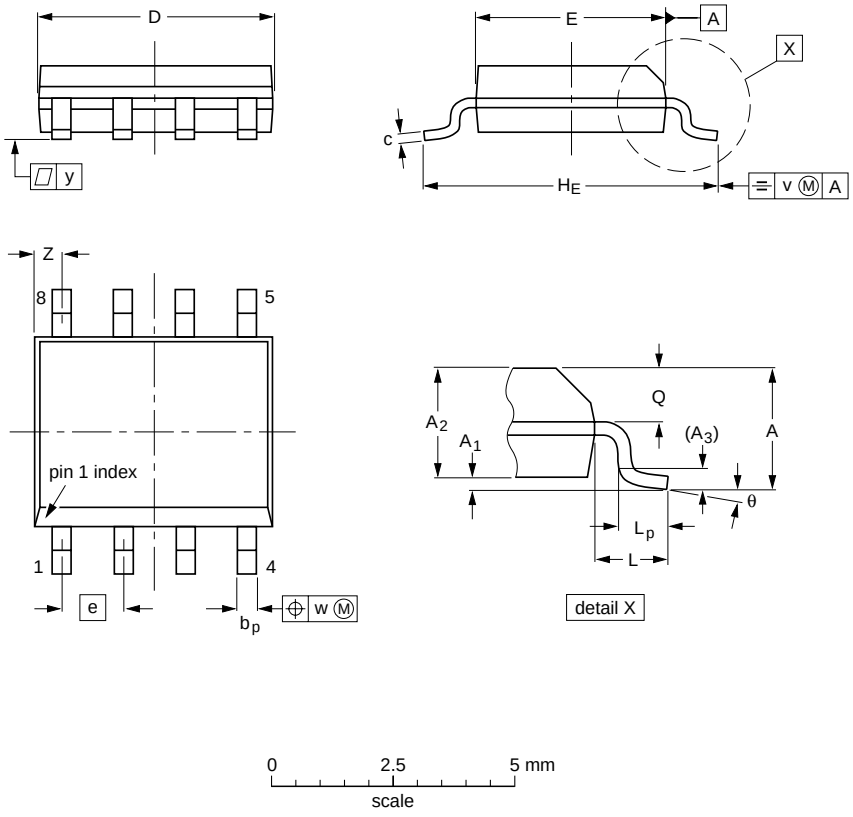
C_L = load capacitance includes jig and probe capacitance

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator

Fig 15. Test circuitry for switching times

13. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

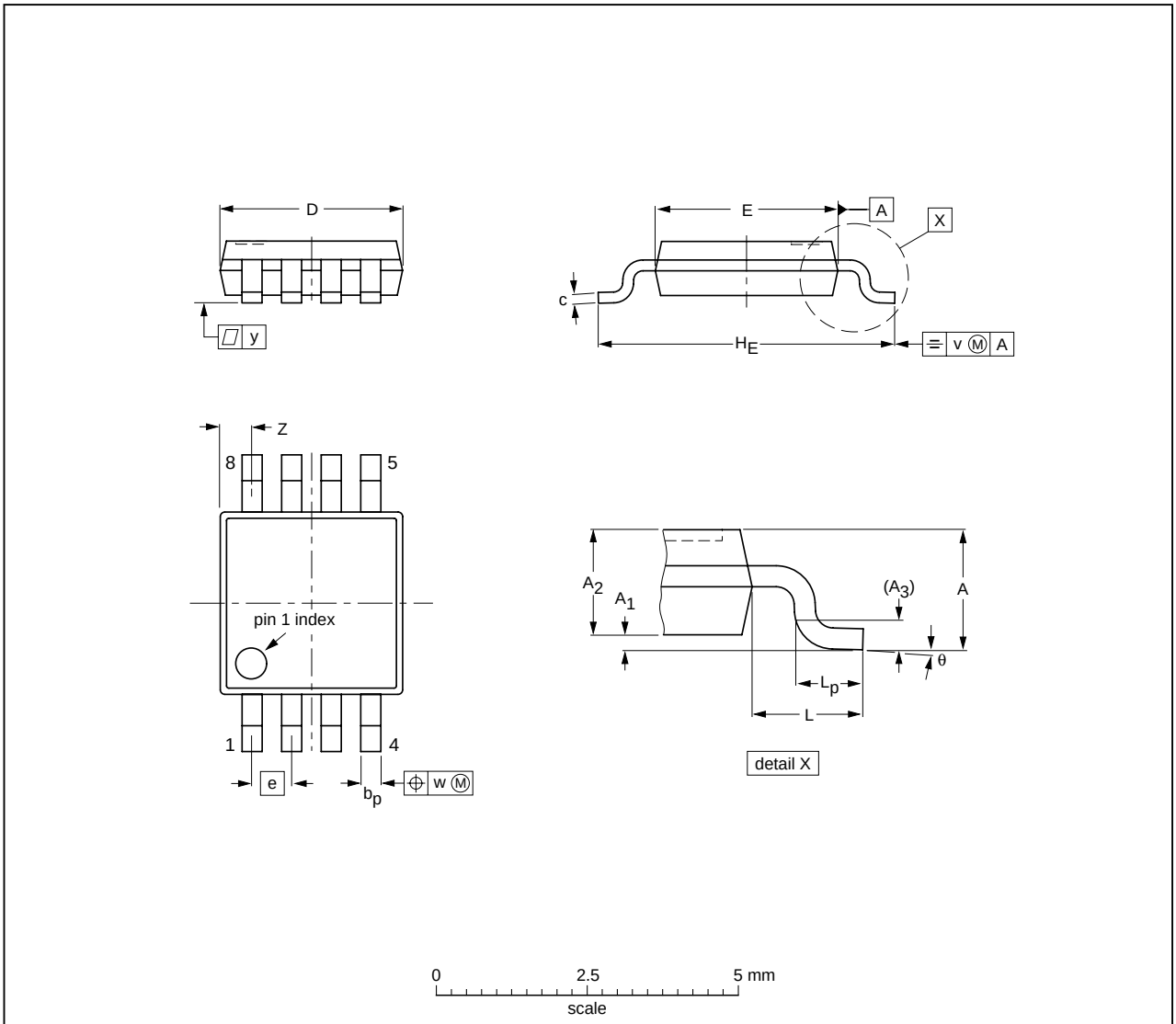
Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 16. Package outline SOT96-1 (SO8)

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

Fig 17. Package outline SOT505-1 (TSSOP8)

14. Soldering

14.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

– smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

14.5 Package related soldering information

Table 6: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	Soldering method	
	Wave	Reflow [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

15. Abbreviations

Table 7: Abbreviations

Acronym	Description
AdvancedTCA	Advanced Telecommunications Computing Architecture
CDM	Charged Device Model
cPCI	compact Peripheral Component Interface
ESD	Electrostatic Discharge
HBM	Human Body Model
I²C-bus	Inter IC bus
MM	Machine Model
PCI	Peripheral Component Interface
PICMG	PCI Industrial Computer Manufacturers Group
SMBus	System Management Bus
VME	VERSAModule Eurocard

16. Revision history

Table 8: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PCA9512A_1	20051007	Product data sheet	-	-	-

17. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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